REMARKS

I. Summary of Preliminary Amendment.

This application is a continuation of parent Application No. 09/899,647, filed July 6, 2001. Claims 1-34 of the present application correspond to previously rejected claims 70-79 and 87-110, respectively, of the parent application.

In this preliminary amendment, applicants amend presently pending independent claims 1, 11, 19, and 27 that directly correspond to the previously rejected independent claims 70, 87, 95, and 103 of the parent application. Applicants have also added new claim 35. In addition to these amendments, applicants address the reasons for patentability in view of the Examiner's remarks in the parent application. No new matter has been added by any of the amendments.

II. Applicants' Specific Amendments and Remarks

a. Presently Pending Claims 1 and 11.

In the parent application, the Examiner cited Purdom, United States Patent 5,750,925, filed October 5, 1994, ("Purdom") as a basis for rejecting applicants' independent claims 70 and 87, which as stated above now correspond to this application's claims 1 and 11 .

Presently, claims 1 and 11 have been amended to distinctly claim and particularly point out that applicants' mounting base subsystem includes "...a plurality of circuit components..." (See e.g., drawing reference numerals 64, 66, 68 70 and 72), "...mounted entirely within said mounting base subsystem...". Nowhere does the Purdom Teach claim or suggest a mounting base subsystem that protects and includes therein the circuit components claimed by applicants. Accordingly, claims 1 and 11 are believed to be in condition for allowance.

b. Presently Pending Claims 19 and 27.

Claims 19 and 27 have been amended in the manner suggested by the Examiner in the Final Action in the parent application. Claims 19 and 27 now distinctly claim and particularly point out that the memory interface chips are "serial/parallel" chips, which, as described in paragraph 51 of the specification, are used to used to convert between "...parallel communications with BGA chips ...and the serial communications path with the processor".

c. New Claim 35.

New claim 35 is presented as a broadened version of Previously allowed claim 80 in the parent application. The

focus of new claim 35 calls for a hardened voyage data recorder, comprising:

(a) a removable memory subsystem;

(b) a mounting base subsystem coupled to said removable memory subsystem; and

(c) a quick release mechanism for uncoupling said memory subsystem from said mounting subsystem.

As discussed with the Examiner in the parent application, this new claim still incorporates a quick release mechanism limitation and is therefore believed, in combination with the other recited elements, to be distinguishable over the cited art which does not teach or fairly suggest the claimed combination. Accordingly, new claim 35 is believed to be in condition for allowance.

d. Applicant's Dependent Claims.

All of this application's dependant claims ultimately stem from independent claims 1, 11, 19, and 27 as such, this application's dependant claims necessarily incorporate all the limitations of their respective independent claims. Therefore, applicant respectfully submits that because independent claims 1, 11, 19, and 27 are

allowable, this application's dependant claims are also allowable.

III. Conclusion

Applicant respectfully submits that claims 1-35 are in condition for allowance. Therefore, this application is in condition for allowance. An early and favorable action is respectfully requested.

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APPENDIX
(Showing How Claim 1, 11, 19, and 27 Have Been Amended)

1. (currently amended) A hardened voyage data recorder, comprising:

(a) a removable memory subsystem;

(b) a mounting base subsystem removably coupled to said memory subsystem, wherein
said mounting base subsystem protects and includes therein electronic circuits, including a plurality of circuit components mounted entirely within said mounting base subsystem, for electronically accessing said memory subsystem.

11. (currently amended) A hardened voyage data recorder, comprising:

(a) a removable memory subsystem; and

(b) a mounting base subsystem, including a plurality of circuit components mounted entirely within said mounting base subsystem, removably coupled to said memory subsystem, wherein

said removable memory subsystem includes non-volatile memory enclosed within a boiler, and
said mounting base subsystem is adapted to be mounted on the exterior of a marine vessel.

19. (currently amended) A hardened voyage data recorder, comprising:

(a) a removable memory subsystem;

(b) a mounting base subsystem removably coupled to said memory subsystem; and

(c) at least one serial/parallel memory interface converter chip coupled to said removable memory subsystem.

27. (currently amended) A hardened voyage data recorder, comprising:

(a) a removable memory subsystem, wherein said removable memory subsystem includes a stacked memory and a plurality of serial/parallel memory interface chips arranged for communication with a processor such that a large number of memory chips may be driven; and

(b) a mounting base subsystem removably coupled to said memory subsystem.